REMARKS

Claims 1-2, 4, 6-10, 13, 15-17, 21-24, 26, and 31-40 are pending in the present application. In the Office Action, claims 34 and 39 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicant respectfully submits that support for the claims 34 and 39 may be found at least at lines 2-8 on page 27 of the specification. Thus, claims 34 and 39 comply with the written description requirement. Applicant requests that the Examiner's rejection of claims 34 and 39 under U.S.C. § 112, first paragraph, be withdrawn.

In the Office Action, claims 1-2, 4, 6-10, 13, 15-17, 21-24, 26, and 31-40 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Wells, et al (U.S. Patent No. 6,687,721), hereinafter referred to as Wells '721, in view of Wells, et al (U.S. Patent No. 6,792,438), hereinafter referred to as Wells '438. The Examiner's rejections are respectfully traversed.

With regard to independent claims 1, 9, 22, 31, and 36, Applicant describes and claims, among other things, a random number generator that includes an entropy register configured to receive a plurality of bits from a corresponding plurality of performance registers. As defined in the specification, performance registers each store a value indicative of a different performance metric. Exemplary performance metrics may include first-level-cache hit rate, second-level-cache hit rate, third-level-cache hit rate, branch target cache, and/or other model specific registers (MSRs), such as those used for measuring performance. In one embodiment, the performance registers include any register that updates the least significant bit at a rate asynchronous to the local and/or system clock. See Patent Application, page 46, l. 23 - page 47, l. 5.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Wells '721 describes an entropy accumulator that may receive one or more random number bits from one or more random bit sources 210. See Wells '721, Figures 2 and 7 and related discussion. The random bit sources 210 comprise circuitry for generating random bits. See Wells '721, col. 4, ll. 34-35 and Figure 4. However, as admitted by the Examiner, Wells '721 does not teach or suggest a random number generator that includes an entropy register configured to receive a plurality of bits from a corresponding plurality of performance registers.

The Examiner alleges that Wells '438 describes a performance register, *e.g.*, a register that updates the least significant bit at a rate asynchronous to the local and/or system clock. Applicants respectfully disagree. Wells '438 describes shift registers 261-264 that are coupled in a serial configuration. However, Wells '438 does not teach that least significant bits of the shift registers 261-264 are updated at a rate asynchronous to the local and/or system clock. To the contrary, conventional shift registers are updated (*i.e.* the bits are shifted) on a rising or falling edge of a clock signal. Thus, Applicants respectfully submit that the prior art of record fails to teach or suggest all of the limitations of the claimed invention.

Moreover, it is respectfully submitted that the cited references fail to provide any suggestion or motivation to modify the prior art to arrive at the claimed invention. To the contrary, both of the cited references appear to teach away from the Examiner's proposed combination and modification of the prior art. First, Wells '721 teaches that random bits should be provided to the entropy register, which teaches away from providing bits related to one or more performance metrics. Second, Wells '438 teaches that a seed for a random number

generator may be generated from bits of data collected from the computer system including the clock. See Wells '438, col. 2, ll. 32-33. Thus, Wells '438 teaches away from using bits that are updated at a rate asynchronous to the local and/or system clock. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Wells '721 in view of Wells '438. Applicants request that the Examiner's rejections of claims 1-2, 4, 6-10, 13, 15-17, 21-24, 26, and 31-40 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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